ECE 448, FPGA Design with VHDL
Spring 2026

Primary Instructor

Dr. Yicheng Zhang <yzhang95@gmu.edu>
The Nguyen Engineering Building, room 3211
In Person Office hours: Tuesday 3:30-4:30 PM, Thursday 3:30-4:30 PM
Zoom Office Hours: by appointment

Lecture

Monday, Wednesday, 01:30-02:45 PM, Blueridge Hall, room 129

Lab Sections and Their Instructors

ECE 448 201: Wednesday, 7:20pm-10pm, Kowsyap Musumuri <kmusumur@gmu.edu>
ECE 448 202: Monday, 9am-11:40am, Ahmad Tahmasivand < atahmasi@gmu.edu >
Grader and New Lab Developer: Diego Alexander Perez Sanchez < dperezs@gmu.edu >

Location of all Lab Sessions: The Nguyen Engineering Building, room 3208
Office hours of all Lab Instructors: see the course canvas page.
Lab sections do not meet in the first week of classes.

Web Page

Canvas -> Spring 2026 FPGA Design with VHDL (ECE-448-001)

Course Description/Overview

Covers the principles and practice of digital hardware design using VHDL. Includes modeling of digital systems for logic synthesis, design flow and tools for FPGAs, verification and testing of designs with testbenches, prototyping on FPGA boards, and examples from communications, control, digital signal processing, and cryptography. Laboratory experiments link simulation to hardware implementation.

Course Learning Outcomes:

By the end of this course, students will be able to design and implement synthesizable digital hardware using VHDL, apply the complete FPGA design flow with industry-standard tools, verify and debug designs through testbenches, simulation, and hardware validation, and prototype and evaluate FPGA-based systems, including implementations drawn from application domains such as digital signal processing, control, communications, and cryptography.

Grading Schema

Percentage Range	Letter Grade
95.00 and above	A+
90.00–94.99	A
85.00–89.99	A−
80.00–84.99	B+
70.00–79.99	B
65.00–69.99	B−
60.00–64.99	C+
50.00–59.99	C
45.00–49.99	C−
40.00–44.99	D
0.00–39.99	F

Grading Weights

Lab assignments:	40%
Lab exercises:	4%
Quizzes & homework:	6%
Midterm exam for the lecture:	10%
Midterm exam for the lab:	15%
Final exam:	25%
Class & Piazza activity:	up to 5% bonus

Grading-related Policies

Assignments (homework and projects) may be submitted up to one week late with a penalty of **25%** of the total points. This means that for a 10-point assignment, the maximum score after the deadline is 7.5 points. No submissions or demos will be accepted **more than one week** after the assignment due date. This policy applies to both individual and group assignments.

Tentative Schedule (subject to modifications):

1. Objectives, Scope, and Organization. 01/21/2026
2. HDL Refresher Quiz. Introduction to Testbenches. 01/26/2026
3. Examples of Testbenches. 01/28/2026
4. Combinational-Circuit Building Blocks. 02/02, 02/04/2026
5. Sequential-Circuit Building Blocks. 02/09/2026
6. Introduction to Basys 3. Using Seven-Segment Displays, LEDs, Switches, and Buttons. 02/11/2026
7. Finite State Machines: State Diagrams, ASM Charts, and VHDL Code. 02/16, 02/18/2026
8. Finite State Machines with Datapath (FSMD). 02/23/2026

9. Implementing Circuits with Regular Structure. 02/25/2026
10. Review for the Midterm Exam. 03/02/2026
11. Midterm Exam. 03/04/2026
12. Introduction to the FPro System. 03/16/2026
13. Bare Metal System Software Development. 03/18/2026
14. Drivers of the LED-MUX Core & Debouncing Core. 03/23/2026
15. Software/Hardware Co-design Using the FPro System - Part 1. 03/25/2026
16. Software/Hardware Co-design Using the FPro System - Part 2. 03/30/2026
17. I/O Register Map of an MMIO Core. Part 1: Exact Address Decoding. 04/01/2026
18. I/O Register Map of an MMIO Core. Part 2: Simplified Address Decoding. 04/06/2026
19. Software/Hardware Co-design Using the FPro System - Part 3. 04/08/2026
20. Programmable Logic Memories. 04/13/2026
21. The FPro Video Subsystem: VGA Display & Frame Buffer Core. 04/15/2026
22. Video cores. 04/20/2026
23. Timing Analysis. 04/22/2026
24. RTL Design Methodology. 04/27, 04/29/2026
25. Review before the Final Exam. 05/04/2026
26. **Final Exam. 05/06/2025, 1:30 pm – 4:15 pm**

Literature

Required Textbooks

Pong P. Chu, *FPGA Prototyping by VHDL Examples: Xilinx MicroBlaze MCS SoC*, Wiley, 2017, 2nd edition.

Supplementary Textbooks

Stephen Brown and Zvonko Vranesic, *Fundamentals of Digital Logic with VHDL Design*, McGraw-Hill, 2008, 3rd edition.

Ricardo Jasinski, *Effective Coding with VHDL: Principles and Best Practice*, The MIT Press, 2016 © 1st edition.

Students with Disabilities

If you need special assistance, please inform the instructor and the Office of Disability Services (ODS, http://ods.gmu.edu) as soon as possible. All special accommodations must be arranged through ODS.

Basic Course Technology Requirements

Activities and assignments in this course will regularly use the Canvas learning system, available at https://mymason.gmu.edu. Students are required to have regular, reliable access to a computer

and a stable broadband Internet connection (cable modem, DSL, satellite broadband, etc., with a consistent 1.5 Mbps [megabits per second] download speed or higher.

Activities in this course will regularly use the web-conferencing software Zoom for office hours. Therefore, students are required to have a device with a functional camera and microphone. In an emergency, students can connect through a telephone call, but video connection is the expected norm.

Academic Integrity

The integrity of the University community is affected by the individual choices made by each of us. Mason has Academic Standards with clear guidelines regarding academic integrity. Three fundamental and rather simple principles to follow at all times are that:

1) all work submitted be your own;
2) when using the work or ideas of others, including fellow students and AI apps, such as ChatGPT, give full credit through accurate citations; and
3) if you are uncertain about the ground rules on a particular assignment, ask for clarification.

No grade is important enough to justify academic misconduct. Plagiarism is the equivalent of intellectual robbery and cannot be tolerated in the academic setting. If you have any doubts about what constitutes plagiarism, please see me.
For more information about the Mason Academic Standards and about the Academic Standards Committee, please visit https://academicstandards.gmu.edu.

AI (Artificial Intelligence) Tools Policy

Consistent with the University Academic Standards Policy, limited and transparent use of AI tools is permitted in this course. Students may use AI tools (e.g., ChatGPT, Copilot, Grammarly, or AI-enabled features in common software) for concept clarification, brainstorming, debugging assistance, or language editing, **but not to generate final solutions, VHDL code, laboratory reports, or exam responses submitted as their own work**. Any use of AI tools must be clearly acknowledged by the student, including the tool used and its purpose. Misuse of AI tools or failure to disclose their use may be treated as a violation of academic integrity.

Common Policies Affecting All Courses at George Mason University

Common policies affecting all courses at George Mason University, including

- the extended information about Academic Standards
- Accommodations for Students with Disabilities
- FERPA and Use of GMU Email Addresses for Course Communication
- Title IX Resources and Required Reporting,

are available at
https://stearnscenter.gmu.edu/home/gmu-common-course-policies
You are strongly encouraged to get familiar with this additional information.