

NVBleed: Covert and Side-Channel Attacks on NVIDIA Multi-GPU Interconnect

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Abstract

Multi-GPU systems are becoming increasingly important in high-performance computing (HPC) and cloud infrastructure, providing acceleration for data-intensive applications, including machine learning workloads. These systems consist of multiple GPUs interconnected through high-speed networking links such as NVIDIA’s NVLink. In this work, we explore whether the interconnect on such systems can offer a novel source of leakage, enabling new forms of covert and side-channel attacks. Specifically, we reverse-engineer the operations of NVLink and identify two primary sources of leakage: timing variations due to contention and accessible performance counters that disclose communication patterns. The leakage is visible remotely and even across VM instances in the cloud, enabling potentially dangerous attacks. Building on these observations, we develop two types of covert-channel attacks across two GPUs, achieving a bandwidth of over 70 Kbps with an error rate of 4.78% for the contention channel. We develop two end-to-end intra-VM side-channel attacks: application fingerprinting (including 18 high-performance computing and deep learning applications) and 3D graphics character identification within *Blender*, a multi-GPU rendering application. These attacks are highly effective, achieving F1 scores of up to 97.78% and 91.56%, respectively. We also discover that leakage surprisingly occurs across Virtual Machines on the Google Cloud Platform (GCP) and demonstrate a side-channel attack on Blender, achieving F1 scores exceeding 88%. We also explore potential defenses such as managing access to counters and reducing the resolution of the clock to mitigate the two sources of leakage.

1 Introduction

Graphics Processing Units (GPUs) have emerged as a primary infrastructure supporting data-intensive applications. These applications range across a number of domains, including machine learning and natural language processing, scientific simulations, cryptocurrency mining, and 3D graphics rendering. As the size of these problems continues to increase, multi-GPU computing is needed to match this expanding demand, which far surpasses the computational and memory resources of a single GPU. For example, training large language models (LLMs) is only possible through large numbers of GPUs: the LLaMA 65B-parameter model leveraged 2048 NVIDIA A100 GPUs across 21 days for its training [56]. Similarly, Smith et

al. [49] trained the Megatron-Turing Natural Language Generation model (MT-NLG) on NVIDIA’s Selene supercomputer, utilizing 560 DGX A100 nodes (several thousand GPUs). Despite the widespread adoption of GPUs across leading cloud computing platforms such as Amazon Elastic Compute Cloud (EC2), Microsoft Azure, and Google Compute Platform (GCP), handling sensitive private information, research into their security remains in its early stages.

To support high-performance multi-GPU applications, multi-GPU systems use custom high-performance interconnects to support the bandwidth and latency requirements of these applications. For example, server-class NVIDIA GPUs leverage high-bandwidth interconnects such as NVLink and NVSwitch to achieve high throughput and low-latency communication. These links are used to communicate between the GPUs either explicitly using commands that copy data from one GPU to another or implicitly through transactions that access shared memory that is mapped to remote GPUs. These communication patterns vary across applications and potentially with the sensitive data processed by applications: if an attacker is able to observe the communication patterns, they may be able to extract sensitive information about the applications and the data they are processing.

A number of previous studies [1, 18, 33, 34, 47, 60, 64, 65] presented covert and side-channel vulnerabilities of a single GPU, or between a Central Processing Unit (CPU) and GPU [12]. One prior work by Dutta et al. [13] proposed a microarchitectural side-channel attack on multi-GPU caches. Our work presents an orthogonal source of leakage that leaks the communication behavior through the multi-GPU interconnect, leaking cross-GPU communication rather than memory access patterns. Our attack also offers advantages in terms of attacker co-location. As a result, the attack substantially expands our understanding of the side-channel threats faced by these systems and the types of defenses needed to mitigate them. Although some prior works have targeted interconnects within the processor chip [12, 42, 57] or the bus interconnect between a CPU and peripherals [47, 53], to our knowledge, this is the first attack to exploit multi-GPU communication.

We reverse-engineer the NVLink behavior and characterize the available sources of leakage that an attacker may exploit. Our investigation reveals that NVIDIA provides user-level accessible performance counters related to NVLink transactions that leak information across applications and even across instances in the real

cloud. In addition, we observe timing differences in the NVLink transactions that leak information about other ongoing communication. Through monitoring these readings, we managed to reverse-engineer the NVLink packet format and communication patterns between multiple GPUs (discussed in § 4). We leverage this leakage to build both covert and side-channel attacks.

We demonstrate attacks on two generations of multi-GPU systems: a local server (DGX-1 system with Tesla P100 GPU) and a public cloud instance (Google Compute Platform with 8 Tesla V100 GPUs), showing the general nature of these attacks. First, we develop two covert-channel attacks (*ContenLink* and *LeakyCounterLink*) in which a sender program on one GPU transmits information covertly to a receiver program on another GPU (discussed in § 5). We optimize the channel by incorporating additional parallelism, attaining a bandwidth of 70.59 Kbps, with an error rate of 4.78% for the contention channel.

We also carry out two end-to-end intra-VM side-channel attacks. In the first attack, we demonstrate that by probing the NVLink performance counters, an attacker can infer the activities of a concurrent application, allowing them to fingerprint applications such as deep learning models and physical dynamics simulation benchmarks (discussed in § 6.1), with 97.8% accuracy. The second attack demonstrates that we can recover data-dependent leakage, identifying which 3D graphics character is being rendered by a victim user running the popular Blender rendering toolkit [7] (discussed in § 6.2), with an accuracy exceeding 91%. We investigated the leakage across different virtual machine instances, which use different GPUs, and discovered, surprisingly, that there is measurable leakage even though the VMs do not communicate. We leverage this leakage to develop a cross-VM side-channel attack on the public cloud platform GCP, achieving an F1 score of over 88% in correctly identifying 3D rendered characters (discussed in § 7). Finally, we discuss the challenges associated with mitigating these attacks and propose potential solutions in § 8.

In summary, the contributions of this paper are:

- We reverse-engineer the NVLink interconnect and identify two leakage sources disclosing aspects of their operation.
- We introduce two types of intra-VM covert-channel attacks that exploit timing and performance counters on two different multi-GPU systems.
- We demonstrate two NVLink-based intra-VM side-channel attacks: (1) fingerprinting applications and (2) identifying 3D graphics character rendering on the victim GPU.
- We identify NVLink leakage across two co-located VM instances and develop a cross-VM side-channel attack capable of identifying 3D graphics characters.

2 Background

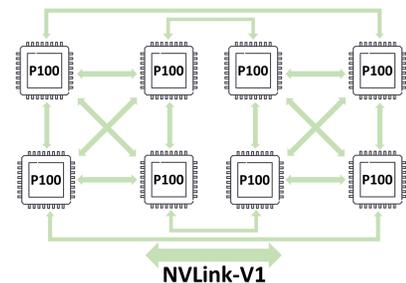
In this section, we provide background on NVLink and an overview of how the GPU performance monitoring unit operates.

2.1 NVLink

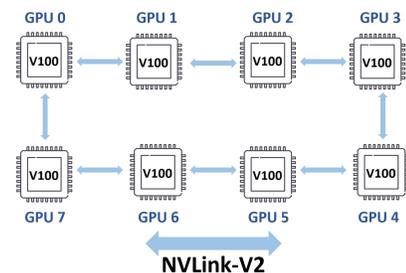
NVLink is a high-speed, high-bandwidth interconnect technology developed by NVIDIA [38] to support data sharing among peer GPUs [30], as well as between CPUs and GPUs. NVLinks are bidirectional, comprising two sublinks, one for each direction. NVLink

supports communication between the GPUs in three different ways: (1) Explicit Peer-to-Peer (P2P) communication enables GPUs to copy data using `cudaMemcpyPeer()`, which copies a user-specified size buffer across the GPUs; (2) Pinned (device) memory, allocated via `cudaMalloc()`, can be accessed by other GPUs without copying it to the host; and (3) Unified virtual memory: in this mode, GPUs are able to access memory that is mapped on remote GPUs. When this happens, either data is migrated at the page boundary or returned at a cache line granularity; these decisions are determined by programmer hints as well as run-time considerations. This permits efficient reading and writing on the remote CPU’s host memory and the device memory of a peer GPU.

NVLink progressed through several generations: NVLink-V1 to V3 and NVSwitch. NVLink-V1 was introduced with NVIDIA’s Pascal P100 GPU [10], featuring 4 NVLink slots per GPU, each achieving a bandwidth of 20 GB/s. NVLink-V2, released with the Volta V100 GPU [6], includes 6 NVLink slots, each with a bandwidth of 25 GB/s. Fig. 1 illustrates the GPU topology of these NVLink generations. NVLink-V3 and NVSwitch are featured in the A100 GPU [5], which is equipped with 12 NVLink links, each with a bandwidth of 50 GB/s. Recently, other GPU manufacturers, excluding NVIDIA, such as AMD, Intel, and others, are beginning to develop a comparable multi-GPU interconnect, the Ultra Accelerator Link (UALink), to compete with NVIDIA’s NVLink [14]. In this study, we conducted experiments encompassing the two generations of NVLink (NVLink-V1 and V2). We leave NVLink-V3 and NVSwitch for future work.



(a) DGX-1 system – P100 GPUs with 4 NVLinks.



(b) GCP 8-GPU machine – V100 GPUs with 6 NVLinks.

Figure 1: GPU topology of two experimental machines.

2.2 GPU Performance Counter

GPU vendors have introduced performance monitoring units, similar to those available on CPUs, to help developers understand and optimize application performance. While these tools provide valuable insights, previous works [24, 34, 44, 47, 54, 59, 60, 62] have shown they can be sources of side-channel leakage. The NVIDIA GPU performance counters are accessed through the CUDA Profiling Tools Interface (CUPTI) [39]. There are a number of NVLink-related performance counters; for instance, `nvlink_total_data_received` tracks the number of bytes of data received across all NVLinks on a particular GPU. AMD also offers analogous APIs for profiling GPU memory and communication transaction metrics [3]. We comprehensively overview all available NVLink-related performance counters in Section 4.2.

3 Threat Model and Attack Overview

In this section, we present our threat model for two attack scenarios based on the placement of the spy and victim. We then summarize the attacker’s capabilities in each scenario and provide an overview of all relevant attacks.

3.1 Threat Model

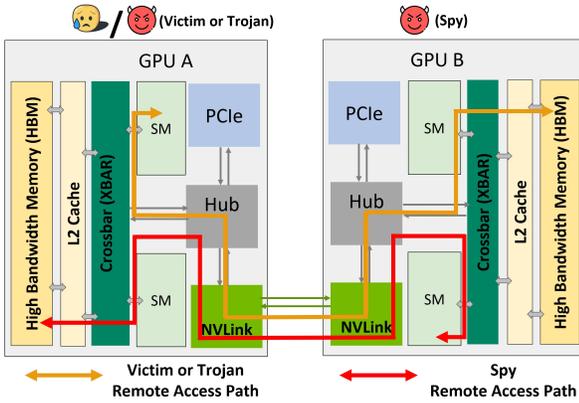


Figure 2: Intr-VM covert and side-channel attacks.

We consider two attack scenarios: (1) Intra-VM attack, where multiple users are co-located on the same GPU system (e.g., NVIDIA DGX) or VM instance on the cloud and share NVLink connections, and (2) Cross-VM attack, where each VM has its own GPU(s), but the GPUs remain interconnected via an unused NVLink.

Intra-VM attack. In this scenario, the attacker and victim reside on different GPUs but share the same NVLink. Fig. 2 provides an overview of this setup. The attacker can exploit two capabilities:

- **Measuring NVLink contention timing:** Without superuser privileges, the attacker can introduce contention on NVLink to observe timing differences, thereby inferring the victim’s behavior.
- **Accessing NVLink performance counters:** NVIDIA supports performance counters that show traffic information on the shared NVLink connections. However, NVIDIA released a driver patch [40] that optionally restricts performance counter access in user mode,

so this leakage vector is only available if this patch is not applied or if the attacker can ask for downgraded drivers to be able to use performance counters. Since performance counters are not reliably available in this threat model, we rely primarily on contention data (the first source of leakage) to estimate the counter values. For example, the counter `nvlink_receive_throughput` can be approximated by continuously transferring a fixed data size and measuring the transfer time:

$$\text{Throughput} = \frac{\text{NVLink_transmission_size}}{\text{Data_transmission_time}} \quad (1)$$

Cross-VM attack. In this scenario, the attacker and victim run on different VMs; however, both VMs’ GPUs share an NVLink connection (see Fig. 12). Due to VM isolation, the attacker cannot directly cause contention with the victim, so there is no timing-based leakage. Nonetheless, major cloud providers (e.g., AWS, GCP, Azure, Alibaba) allow users to install any version of GPU drivers. Consequently, the attacker can downgrade her VM’s driver to enable performance counter collection, while the victim does not need to downgrade. By doing so, the attacker can infer the victim’s NVLink transactions, even across VMs.

3.2 Overview of Attacks

Intra-VM covert channel attack. We introduce two types of intra-VM covert channel attacks: *ContenLink* and *LeakyCounterLink*. We assume the sender and receiver processes run on separate GPUs in both cases. In *ContenLink*, we exploit NVLink contention leakage to establish a covert channel between two GPUs. In *LeakyCounterLink*, we exploit NVLink leaky counters to demonstrate a covert channel attack (please note the potential access limitations to this leakage described above). We evaluate the effectiveness of these attacks using two metrics: bandwidth and error rate.

Intra-VM side-channel attack. Next, we present two end-to-end intra-VM side-channel attacks. In both attacks, the victim and attacker processes run on two different GPUs but share the same NVLink. The first demonstrates application fingerprinting across 18 different applications. The second showcases 3D character fingerprinting using 50 characters from Blender Studio [8]. To assess the performance of these classifiers, we calculate three metrics: F1 score (F1), Precision (Prec), and Recall (Rec).

Cross-VM side-channel attack. Finally, we demonstrate an end-to-end cross-VM side-channel attack. We assume the attacker and victim reside in separate VMs connected via an unused NVLink. Here, the attacker aims to identify which 3D characters are being rendered in the victim’s VM. The same feature extraction and evaluation metrics from our earlier side-channel attacks are applied in this scenario as well.

4 Demystifying NVLinks

In this section, we first reverse-engineer the NVLink operation. Next, we analyze the NVLink-related performance counters and identify their leakage. Finally, we study the timing behavior when NVLink contention arises to identify timing-related leakage.

Experiment platform. We use a local DGX-1 multi-GPU system as well as a public cloud server from Google as our experimental environments (details in Table 1). Fig. 1 presents an abstract view of the NVLink topology in these systems. The DGX-1 system employs

a hypercube topology, while the GCP 8-GPU platform uses a ring topology. We tested the GCP VMs in three different regions: us-central1-c, us-east1-c, and us-west1-a.

Table 1: Specification of two target platforms.

	DGX-1 system	Server (GCP)
CPU	Intel Xeon E5-2698v4	GCP N1-standard
Memory	256GB	100 GB
GPU	8 Tesla P100s	8 Tesla V100s
OS	Ubuntu 22.04	Ubuntu 20.04
CUDA	V12.2	V10.1.243
GPU driver	535.129.03	525.125.06
NVLink version	NVLink-V1	NVLink-V2
NVLink slots	1 for peer GPUs	3 for peer GPUs

4.1 Reverse Engineering NVLink Operation

NVLink operates as a packet-based interface, where each packet can contain multiple Flow Control Units (flits). Fig. 3 illustrates the format of an NVLink packet. In this section, we use NVLink-related counters to reverse-engineer NVLink characteristics, such as the packet format.

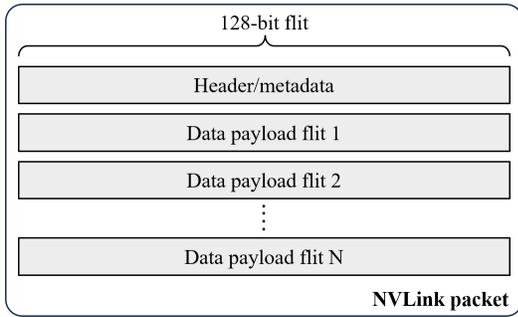


Figure 3: NVLink-V1 packet format.

NVLink-V1 (DGX-1 system). As discussed in an NVIDIA whitepaper [17], NVLink-V1 utilizes a uniform packet format comprising a header, metadata, and $N = 16$ data payload flits. Each flit is 128 bits (16 bytes), enabling the transfer of $16 \times N = 256$ bytes of data per NVLink packet. The minimum data transmission size on NVLink-V1 is 32 bytes, corresponding to 2 data payload flits.

NVLink-V2 (GCP V100). However, the packet format for NVLink-V2 has not been documented. Therefore, we design experiments to reverse-engineer this format. Specifically, we initiate data transfers from GPU 1 to GPU 0 via NVLink using `cudaMemcpyPeer()`, varying the size of the data transferred. Concurrently, we profile the counter `nvlink_user_data_received` on GPU 0. This counter is chosen because it excludes headers and metadata, accurately monitoring the NVLink data transmission size.

Fig. 4 illustrates the usage of data flits with an increasing number of data transmissions on NVLink-V2 (GCP V100 machine). We obtain 3 separate readings as GPUs 0 and 1 in GCP machines are equipped with 3 NVLink slots. As depicted in Fig. 4 (b), we observe 8

distinct steps for every 256 bytes. We notice that the 3 NVLink slots are sequentially activated as the data transmission size increases. For example, when the data transmission size is less than 256 bytes, only slot 1 (indicated in blue) is activated, while the other two slots remain idle. However, when the data size exceeds 256 bytes, slot 2 (indicated in yellow) is also engaged to handle the additional data transfer. Thus, this observation leads us to conclude that the maximum packet size for NVLink-V2, consistent with NVLink-V1, is 256 bytes, comprising 16 data payload flits.

Furthermore, Fig. 4 (a) depicts a zoomed-in view of the first NVLink packet. In the first NVLink packet, we observe 8 steps for every 32 bytes, corresponding to the size of 2 data flits, indicating that the size of the packet is increased at a granularity of 2 flits. For example, we note that slot 1 (indicated in blue) uses 2 data flits (32 bytes), even when the data transfer size is less than 32 bytes, which appears to be the smallest transaction size.

Observation 1: *The minimum data transmission size for both NVLink-V1 and NVLink-V2 is 32 bytes, equivalent to 2 data payload flits, and increases with a two-flit granularity. Each NVLink-V1/V2 packet contains a maximum of 16 data payload flits, totaling 256 bytes. Transmissions use the available sublinks concurrently when possible although the pattern is not consistent.*

4.2 NVLink Performance Counters

We collect all NVLink-related counters from CUPTI and evaluate them for potential leakage: Table 2 summarizes the 14 NVLink-related counters.

Experiment 1: Receive vs transmit. All NVLink counters feature both `receive` and `transmit` attributes. According to NVIDIA’s white paper [17], an NVLink transaction begins with a request from the requester GPU, followed by the target GPU transmitting the data payloads back to the requester. The request consists only of metadata describing the requested data, making it significantly smaller than the payloads transmitted from the target GPU. We profile all NVLink counters by transmitting varying-sized packets using `cudaMemcpyPeer()`. We observe that on GPU 0 (receiver GPU), the `receive` counters consistently show significantly higher values than the `transmit` counters. Therefore, by examining NVLink `receive/transmit` values, the attacker can determine the victim’s data transfer direction.

Observation 2: *The NVLink `receive/transmit` attributes reveal NVLink data transaction direction.*

Experiment 2: User vs total. We observed that, aside from throughput, all categories feature both `user` and `total` attributes; these attributes are undocumented, so we explore them using the following experiment.

In this experiment, a spy program continuously transfers data from GPU 0 to GPU 1 while profiling NVLink’s `user` and `total` counters. Concurrently, we execute a program with a known NVLink communication pattern and observe the performance counters; in this experiment, we use a 3D rendering tool, Blender, to render 5

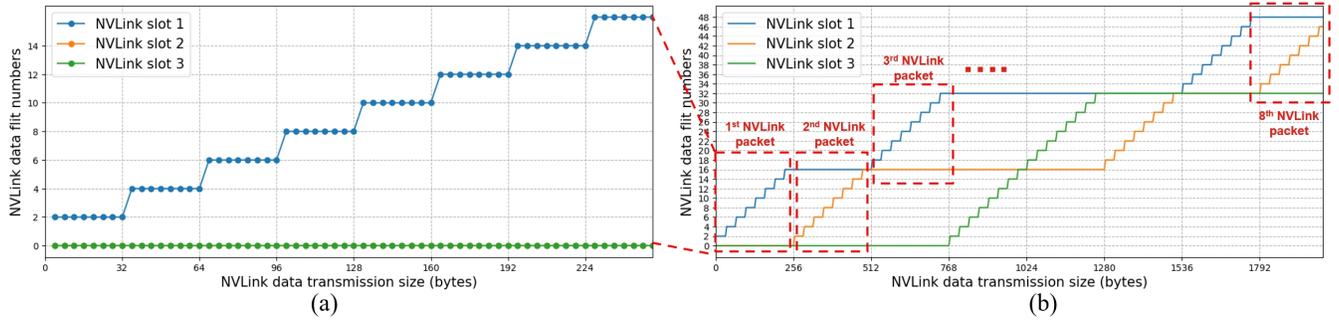


Figure 4: Reverse engineering NVLink transmission (NVLink-V2): (a) First packet, sizes 0–256 bytes, (b) Multiple packets.

Table 2: NVLink-related performance counters, available from NVIDIA CUPTI [39].

Category	Counter Name
Throughput	nvlink_receive/transmit_throughput
User	nvlink_user_data_received/transmitted, nvlink_user_write_data_transmitted, nvlink_user_response_data_received
Total	nvlink_total_data_received/transmitted, nvlink_total_response_data_received, nvlink_total_write_data_transmitted
Atomic operation	nvlink_total/user_nratom_data_transmitted, nvlink_total/user_ratom_data_transmitted

frames. Blender transfers 3D object data in each frame using the shared NVLink. As Fig. 5 shows, user counters remain unaffected. However, the total counters aggregate the transaction data from all programs using a shared NVLink. The 5 NVLink transmissions from Blender are clearly visible to the spy program. Therefore, by measuring the total NVLink values, the attacker can estimate the victim’s data transmission size.

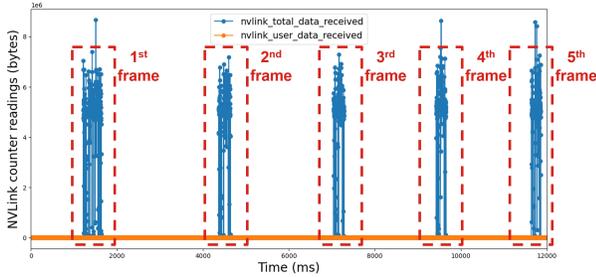


Figure 5: Counter traces for five consecutive frames.

Observation 3: When NVLink is shared, the NVLink total counters reveal all data transaction patterns, including those from other users.

Experiment 3: Aggregation mode. As illustrated in Fig. 1, P100 GPU (NVLink-V1) and V100 GPU (NVLink-V2) are equipped with 4 and 6 NVLink slots, respectively. NVLink offers an aggregate mode for performance counters that may be disabled [41]. We discovered that when aggregation mode is turned off, the counters detail the data transaction sizes for each individual NVLink slot. In the DGX-1 system, we obtain 4 values per GPU, each corresponding to one link. In contrast, for the GCP setup, we receive 6 values per GPU.

Observation 4: When aggregation mode is off, counter values are available for individual NVLink slots, providing finer-grain leakage.

NVLink counter selection. As a result of these experiments, we identify two counters, `nvlink_total_data_received` and `nvlink_total_data_transmitted`, to use in our attacks. We rule out user counters since they do not leak information, while total counters leak transmitted data information regarding other applications. In addition, we observed that throughput counters incur higher overhead, limiting the rate of obtaining information. Finally, the counters tracking atomic operations remain zero for applications that do not use remote atomic operations, limiting their utility.

4.3 Timing-Based Leakage Due to Contention

The final set of reverse engineering experiments targets timing properties under contention. Contention occurs when multiple components simultaneously access shared resources, such as buses or I/O ports, which are constrained by bandwidth or capacity limits. In our threat model (Fig. 2), the victim program is on GPU A, and the spy program is on GPU B. The victim accesses data from GPU B via NVLink while the spy fetches data from GPU A, leading to contention on the Crossbar (XBAR), High-speed Hub (HSHUB), and NVLink I/O ports. The XBAR enables data exchange between GPU SM cores, L2 cache, and high bandwidth memory (HBM) [36]. The HSHUB connects the XBAR to the GPU’s I/O ports (PCIe or NVLink) [37]. As they contend for these resources, this concurrent use of the NVLink from both programs results in observable delays compared to when the link is idle.

We use two programs in our experiments: (1) Program A, which continuously measures execution time in clock cycles using the RDTSCP instruction [25]. It does so for each `cudaMemcpyPeer()` execution (initiated by the CPU) that transfers 256 bytes (a single

packet) via NVLink. (2) Program **B**, which transfers varying sizes of data over the shared NVLink, either explicitly via `cudaMemcpyPeer()` or implicitly through Unified Virtual Memory. We conduct experiments on both DGX-1 (NVLink-V1) and GCP machines (NVLink-V2).

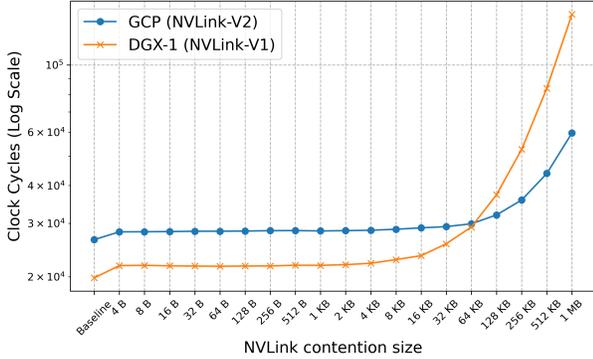


Figure 6: NVLink contention measurements.

Contention size effect. Fig. 6 illustrates the impact of contention size on both NVLink-V1 and NVLink-V2 when program **B** transfers data through NVLink explicitly using `cudaMemcpyPeer()`. When two programs share the NVLink, even a data transfer as small as 4 bytes can introduce a measurable delay exceeding 10%. As the contention size increases, we observe a corresponding increase in timing delay. When the contention data size exceeds 256 bytes, both NVLink-V1 and NVLink-V2 experience consistent and noticeable contention delays.

We also observe that the interconnect topology in multi-GPU systems significantly impacts contention. As illustrated in Fig. 2, a DGX system (NVLink-v1) connects two P100 GPUs via a single NVLink slot, while Google Cloud Platform (NVLink-v2) connects two V100 GPUs via three NVLink slots. Our measurements (see Fig. 6) show that single-slot configurations are more prone to contention than multi-slot setups.

Observation 5: NVLink contention leads to observable increases in data transfer time.

Summary of identified NVLink leakages. Observations 2, 3, and 5 reveal that NVLink performance counters, although not intended for this purpose, aggregate data transaction patterns from all users on the shared NVLink, which can be exploited. These patterns include transfer sizes, directions, and timings, which an attacker can use to infer a victim’s behavior. Specifically:

- Observation 2: By examining NVLink receive/transmit values, an attacker can determine the victim’s data transfer direction.
- Observation 3: By tracking NVLink total counters, an attacker can estimate the size of the victim’s transactions.
- Observation 5: By introducing NVLink contention, an attacker can exploit a timing-based side channel to gather further information about the victim’s activities.

5 Intra-VM Covert-Channel Attacks

We explore two designs of covert channels: *ContenLink* and *LeakyCounterLink*. *ContenLink* is based on timing variations due to contention effects on the shared links. *LeakyCounterLink* exploits NVLink’s leaky performance counters.

5.1 Covert-Channel Design

This section describes the design of the two covert channels. Important to covert channels is the ability of the sender and receiver to synchronize, which we describe first.

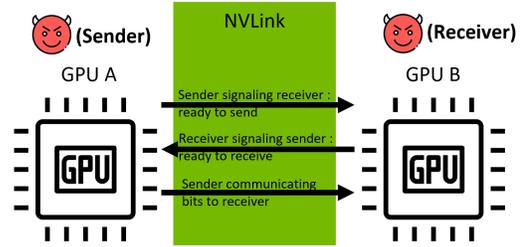


Figure 7: Synchronization protocol for covert channels.

Synchronization. Synchronization is essential for improving the bandwidth and controlling the error rate on a covert channel. Fig. 7 illustrates the synchronization process which is conducted in three phases. The sender begins the handshake by transmitting a pre-agreed data pattern through NVLink, thereby signaling its readiness to send. Upon detecting this signal via GPU performance counters, the receiver program acknowledges its readiness to receive by reciprocating with a data transfer of equivalent size back to the sender’s GPU. This completes the second step of the handshake. Once the handshake is successfully concluded, the sender proceeds to transmit the covert data bits to the spy program.

Design 1: ContenLink. As we observed in Section 4, contention on a shared NVLink leads to an increase in data transfer time. We build a covert channel that exploits this timing difference to transmit data covertly. Algorithm 1 outlines the design of the *ContenLink* receiver. Initially, the receiver allocates two 256-byte arrays, R_0 in the local GPU 0 and R_1 in the remote GPU 1, respectively. We set the array size to 256 bytes because, based on our first observation, this is the maximum size of a single NVLink packet. The receiver measures the execution time for invoking the `cudaMemcpyPeer()` API, which facilitates the copying of arrays R_1 to R_0 via NVLink, using the hardware timer accessible through the RDTSCP instruction. If the measured time falls below a threshold T , the receiver interprets this as free of contention on the NVLink, indicating a received bit of ‘0’. Conversely, a measurement exceeding the threshold signifies contention, interpreted as a received bit of ‘1’.

Algorithm 2 presents the sender’s design for the covert channel. The initial step involves allocating two arrays, S_0 and S_1 , on two GPUs. The differing sizes of these arrays are intended to exert varying levels of contention pressure on the NVLink. We evaluate the impact of varying sender sizes on the covert channel’s bandwidth and error rate in Section 5.2. After synchronizing with the receiver, the sender starts the transmission of covert messages. To transfer a

Algorithm 1: Receiver for ContenLink Covert Channel

```
//  $D_{\text{receive}}[N]$  is an array of  $N$  bits to receive a message;
//  $T$  is the threshold to distinguish between bits '1' and '0';
Allocate an array  $R_0$  in local GPU 0's memory;
Allocate an array  $R_1$  in remote GPU 1's memory;
Synchronization();
for  $i \leftarrow 0$  to  $N - 1$  do
  Record time  $start$  via RDTSCP;
  Execute cudaMemcpyPeer() to copy  $R_1$  to  $R_0$ ;
  Record time  $end$  via RDTSCP;
  if  $end - start < T$  then
    |  $D_{\text{receive}}[i] \leftarrow 0$ ;
  else
    |  $D_{\text{receive}}[i] \leftarrow 1$ ;
  end
end
```

bit '1', it uses `cudaMemcpyPeer()` API to copy S_1 to S_0 from remote GPU to local GPU, creating contention on the shared NVLink with the receiver. For transmitting a bit '0', it performs K loops of NOP instructions, which does not cause contention on the NVLink.

Algorithm 2: Sender for Covert Channel

```
//  $D_{\text{sender}}[N]$  is an array of  $N$  bits used to send a message;
//  $K$  is the number of execution of NOPs;
Allocate an array  $S_0$  in local GPU 0's memory;
Allocate an array  $S_1$  in remote GPU 1's memory;
Synchronization();
for  $i \leftarrow 0$  to  $N - 1$  do
  if  $D_{\text{receive}}[i] == 1$  then
    | Execute cudaMemcpyPeer() to copy  $S_1$  to  $S_0$ ;
  else
    for  $j \leftarrow 0$  to  $K - 1$  do
      | Execute a NOP;
    end
  end
end
```

Design 2: LeakyCounterLink. Based on our second and third observations, we develop an alternative design for an intra-VM covert channel. By monitoring two NVLink counters: `nvlink_total_data_transmitted` and `nvlink_total_data_received`, the receiver can observe not only its own data transfer patterns but also those of the sender. Algorithm 3 shows the design of the receiver. Similar to *ContenLink* receiver, it also allocates two 256-byte arrays: one on local GPU 0 and the other on remote GPU 1. After synchronizing with the sender, the receiver continuously profiles two NVLink counters while executing the `cudaMemcpyPeer()` API. If the counter values are less than the threshold T , it records a bit of '0'. Otherwise, a bit of '1' is stored in the receiver's array.

5.2 Covert Channel Evaluation

In this section, we evaluate two designs of intra-VM covert-channel attacks on both DGX-1 system and GCP machines.

Evaluation of *ContenLink*. To evaluate *ContenLink*, we transmitted a 10,000-bit message five times and calculated the average

Algorithm 3: Receiver for LeakyCounterLink Covert Channel

```
//  $D_{\text{receive}}[N]$  is an array of  $N$  bits used to receive a message;
//  $T$  is the threshold to differentiate bits '1' and '0';
Allocate an array  $R_0$  in local GPU 0's memory;
Allocate an array  $R_1$  in remote GPU 1's memory;
Synchronization();
for  $i \leftarrow 0$  to  $N - 1$  do
  cudaProfilerStart();
  Execute cudaMemcpyPeer() to copy  $R_1$  to  $R_0$ ;
  cudaProfilerStop();
  Record NVLink leaky counters value to  $counter$ ;
  if  $counter < T$  then
    |  $D_{\text{receive}}[i] \leftarrow 0$ ;
  else
    |  $D_{\text{receive}}[i] \leftarrow 1$ ;
  end
end
```

bandwidth and error rate. The error rate was determined using the Levenshtein edit distance [32]. Each message, composed of an equal number of '0' and '1' bits, was randomly generated. Fig. 8 and Fig. 9 illustrate the bandwidth and error rate on two platforms. Based on our contention measurements detailed in Section 4.3, the varying data pressures exerted by the sender distinctly affect the covert channel's performance. We tested sender data sizes ranging from 256 bytes to 4 MB. We ignore sizes smaller than 256 bytes because we find that when the contention size is small, it becomes challenging for the receiver to distinguish between bit '1' and '0', resulting in a high error rate. On the GCP machine, we achieved the highest bandwidth of 70.59 Kb/s with a sender data size of 256 bytes, accompanied by an error rate of 4.78%. Similarly, on the DGX-1 machine, the highest bandwidth reached was 60.71 Kb/s with the same sender data size, resulting in a lower error rate of 1.86%. As the data pressure from the sender increases, we observe a corresponding decrease in the bandwidth of covert channels on both GCP and DGX systems, although the error rate remains stable.

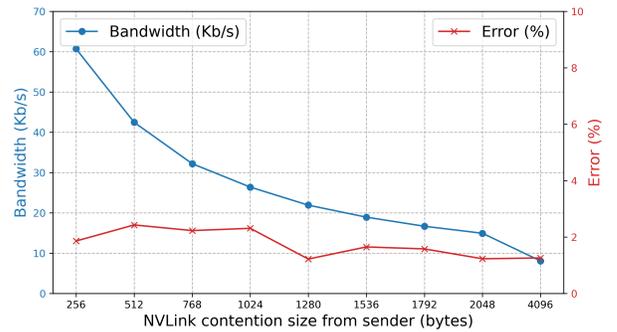


Figure 8: DGX contention covert channel results.

Evaluation of *LeakyCounterLink*. We employed the same evaluation methods for *LeakyCounterLink* as were used for *ContenLink*. However, its performance was inferior to that of *ContenLink*. On the GCP platform, the highest bandwidth achieved was 1.88 Kb/s with a

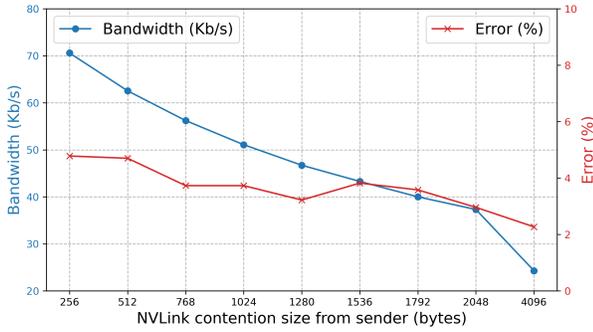


Figure 9: GCP contention covert channel results.

sender data size of 256 bytes, accompanied by an error rate of 7.50%. Similarly, on the DGX-1 machine, the highest bandwidth recorded was 1.39 Kb/s with the same sender data size, resulting in an error rate of 8.80%. When we use CUPTI to profile leaky counters, the CUPTI profiler introduces significant overhead. This is due to the need for synchronization of profiling resources between the host and the device, as well as the delivery of activity buffers to the client via the buffer completed callback [39]. Consequently, this overhead adversely affects the bandwidth of *LeakyCounterLink*. Additionally, although the leaky counters can profile the transaction behavior of other users, they are unstable and noisy. This instability contributes to a higher error rate compared to *ContenLink*.

6 Intra-VM Side-Channel Attacks

In this section, we demonstrate two end-to-end side-channel attacks: application fingerprinting and 3D object fingerprinting attacks.

6.1 Attack 1: Application Fingerprinting

In this attack, we reveal that an adversary can infer the specific HPC applications or deep learning models by exploiting NVLink side-channel leakages. We test application fingerprint attacks on 8 HPC applications from the OpenMM [15] benchmarks and 10 deep-learning models as the victim applications.

OpenMM benchmark. OpenMM is a high-performance toolkit tailored for molecular dynamics simulations, supporting multi-GPU systems. In this study, we center our attention on 8 benchmark applications [55]: *rf*, *pme*, *apoa1-rf*, *apoa1-pme*, *apoa1-ljpme*, *amoeba-pme*, *amber20-dhfr*, and *amber20-cellulose*.

Deep learning models. In this work, we consider the attacker’s attempts to extract the model structure like in previous work [13, 34, 53, 60]. Specifically, we select 10 popular deep learning models (5 simple and 5 complex). The simple models include a Multi-layer Perceptron (MLP), two basic Convolutional Neural Networks (CNNs), a regression model, and a Long Short-Term Memory (LSTM) network [22]. For the complex models, we chose 5 famous models: AlexNet [29], VGG16 [48], GoogLeNet [52], and two variants of ResNet (ResNet-18 and ResNet-50) [21] used in Computer Vision (CV). Each model was trained on the MNIST dataset [11], utilizing PyTorch-supported data parallelism for distributed training across

100 iterations [43]. The batch size was set at 64. For complex models, the image size was resized to 224 by 224. We leave the layer hyper-parameter extraction as future work.

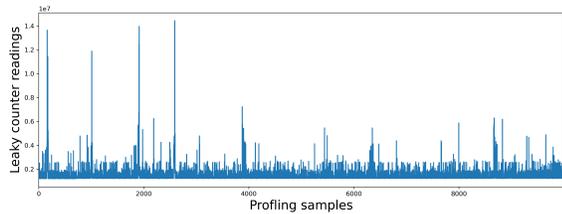
Experimental setup and data collection. We assume the victim deploys her application using three different GPU distribution strategies, with 2, 4, or 8 GPU configurations. The spy application continuously monitors the side-channel leakages from a single NVLink utilized by the victim. The background spy program was set up to profile the counter values: `nvlink_total_data_received`, along with timing delays caused by the victim application’s contention on NVLink. As outlined in Section 4.2, we turn off the aggregation mode of the profiler and collect leakage for each individual link. Consequently, for the DGX-1 platform, which encompasses 4 NVLink-V1 slots per GPU, the spy program collects 5 leakage vectors, encompassing 4 vectors for links and timing delay information. Similarly, with the GCP platform, which features 6 NVLink-V2 slots per GPU, attackers can acquire 7 leakage vectors. This includes 6 vectors from links and timing delay. During the data collection phase, we collected 50 traces of side-channel leakages for each application. The dataset was divided into training and testing sets using an 80/20 split ratio.

Observing benchmark distinguishability. Fig. 10 displays traces for 4 applications—*rf*, *amber20_cellulose*, AlexNet and ResNet-50—highlighting their distinguishable characteristics. The numbers on the X-axis correspond to the profiling samples. The Y-axis displays the leaky counter readings; in this case, we use `nvlink_total_data_received` in bytes.

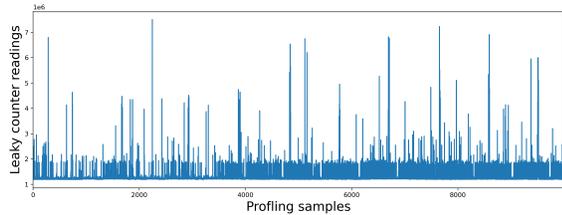
Feature engineering and classification. We extract features from the collected time-series data. We use a sliding window approach with a window size of 100 to compute 12 statistical features listed in Table 3. We then use the extracted features to build classification models, employing three standard machine learning algorithms: K Nearest Neighbors (KNN) [28] with parameter settings: $n_neighbors = 5$, $leaf_size = 30$, XGBoost [4] with parameter settings: $n_estimators = 100$, $max_depth = 6$, and Light Gradient Boosting Machine (LightGBM) [27] with parameter settings: $num_leaves = 31$, $max_depth = -1$, $n_estimators = 100$. To assess the performance of these classifiers, we calculated three metrics [23], including the F1 score (F1), Precision (Prec), and Recall (Rec).

Table 3: Definitions of statistical features used in *NVBleed*.

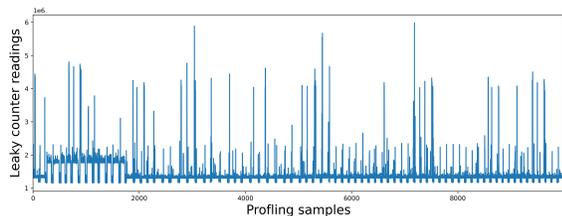
Features	Description
mean	Mean of all values.
max	Maximum of all values.
min	Minimum of all values.
median	Median of all values.
std	Standard deviation.
var	Variance.
range	Difference of maximum and minimum.
sum	Sum of all values.
count_am	Count of observations that exceed the mean.
percent_25	25th percentile value.
percent_75	75th percentile value.
iqr_val	Interquartile range.



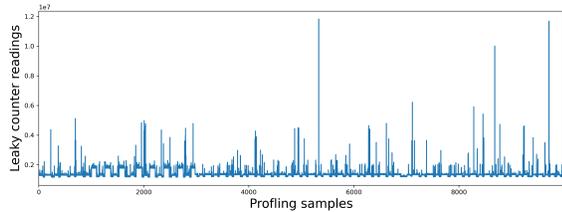
(a) The NVLink leakage traces of rf.



(b) The NVLink leakage traces of amber20_cellulose.



(c) The NVLink leakage traces of AlexNet.



(d) The NVLink leakage traces of ResNet-50.

Figure 10: Comparison of NVLink leakage traces.

Results. We evaluated the application fingerprinting attack under two attacker capabilities: (1) **Timing only**: exploiting contention-based timing leakage on NVLink, and (2) **Timing + Counters**: combining timing leakage with leaky performance counters. This second attack is only possible if the performance counters are enabled in the GPU driver. For 2-GPU configurations, Table 4 presents the classification performance results. XGBoost and LightGBM achieve the highest accuracy on the DGX testbed and GCP machine, with F1 scores exceeding 82% and 96%, respectively, using only timing leakage. Incorporating leaky performance counters alongside timing leakage further improves classification performance, achieving F1 scores above 92% and 97% for the DGX testbed and GCP machine, respectively. For 4-GPU configurations (Table 5), under timing leakage alone, LightGBM delivers the best performance on DGX (F1 = 88.04%), while XGBoost narrowly leads on GCP (F1 = 89.17%). Once performance counters are combined with timing leakage, XGBoost

becomes the top performer on both platforms, surpassing 95% F1 on DGX and 88% on GCP. In 8-GPU configurations (Table 6), with timing leakage only, LightGBM attains the highest F1 score on both DGX (82.27%) and GCP (73.41%). Incorporating leaky performance counters further increases LightGBM’s scores to 90.91% on DGX and 85.40% on GCP.

As the multi-GPU system topology becomes more complex with additional GPUs, the overall accuracy of the classifiers decreases. However, combining contention-based timing signals with performance counter data significantly enhances classification accuracy while maintaining strong attack performance, with F1 scores consistently exceeding 85%.

Table 4: Application fingerprint performance: F1 (%), Precision (%), and Recall (%) on DGX and GCP (2 GPUs). $\textcircled{1}$ = Contention-based timing leakage, $\textcircled{1} + \text{⊞}$ = Leaky performance counters.

		DGX			GCP		
		F1	Prec	Rec	F1	Prec	Rec
$\textcircled{1}$	KNN	36.22	37.26	39.44	55.77	55.97	58.89
	XGBoost	82.69	82.95	82.78	96.65	96.90	96.67
	LightGBM	81.21	81.25	81.67	96.77	97.23	96.67
$\textcircled{1} + \text{⊞}$	KNN	25.96	31.45	26.11	55.77	55.97	58.89
	XGBoost	90.87	91.45	91.11	97.78	98.06	97.78
	LightGBM	92.22	93.12	92.22	96.10	96.93	96.11

Table 5: Application fingerprint performance: F1 (%), Precision (%), and Recall (%) on DGX and GCP (4 GPUs). $\textcircled{1}$ = Contention-based timing leakage, $\textcircled{1} + \text{⊞}$ = Leaky performance counters.

		DGX			GCP		
		F1	Prec	Rec	F1	Prec	Rec
$\textcircled{1}$	KNN	54.20	58.26	57.22	66.65	69.16	67.78
	XGBoost	85.77	86.51	85.56	89.17	89.56	89.44
	LightGBM	88.04	88.64	87.78	89.05	89.36	89.44
$\textcircled{1} + \text{⊞}$	KNN	21.67	23.73	24.44	63.26	66.50	64.44
	XGBoost	95.43	95.70	95.56	88.60	89.79	88.60
	LightGBM	92.64	93.20	92.78	88.14	89.08	88.33

Table 6: Application fingerprint performance: F1 (%), Precision (%), and Recall (%) on DGX and GCP (8 GPUs). $\textcircled{1}$ = Contention-based timing leakage, $\textcircled{1} + \text{⊞}$ = Leaky performance counters.

		DGX			GCP		
		F1	Prec	Rec	F1	Prec	Rec
$\textcircled{1}$	KNN	42.38	47.09	44.44	63.01	66.60	63.33
	XGBoost	79.30	79.40	79.44	71.54	71.71	72.78
	LightGBM	82.27	82.88	82.22	73.41	74.32	73.89
$\textcircled{1} + \text{⊞}$	KNN	23.51	28.83	25.56	66.36	69.96	66.67
	XGBoost	89.46	90.31	89.44	84.51	85.98	85.00
	LightGBM	90.91	92.34	91.11	85.40	86.10	86.11

6.2 Attack 2: Identifying Rendered Characters

We demonstrate a proof-of-concept attack that a spy application can identify which 3D production character the victim is rendering. We begin by providing background on how the Blender renders 3D characters. Following this, we outline our attack methodology and discuss the evaluation results.

3D character rendering on multi-GPU. 3D scene rendering is an intensive process utilized to generate images and movies from scenes modeled in specialized software environments, such as Blender [7], Unity [20], Unreal Engine [19], and others. Utilizing GPUs to accelerate 3D rendering has become a standard practice within these toolkits [26]. The initial step in rendering 3D scenes with GPU assistance involves transferring scene data from CPU to GPU memory. After the computation is completed, the rendered data is transferred back to the CPU to finish rendering. In this study, we choose Blender as the target 3D rendering toolkit for two main reasons: first, its widespread use and open-source nature; second, its support for accelerated rendering on multiple GPUs through NVLink. By activating the "Distribute Memory Across Devices" option on the Blender, the 3D scene data are not duplicated across each GPU. Instead, this data is transferred to a single GPU from the CPU via PCIe. Subsequently, all NVLink-connected GPUs can share the scene data efficiently. This approach significantly enhances the speed of rendering complex and massive scenes.

Observing 3D graphics character distinguishability. Fig. 5 depicts the NVLink counter readings for 5 consecutive frames. These readings clearly show the start and end times of rendering for each frame. When zoomed in, as illustrated in Fig. 11, we observe that the renderings of two 3D characters (Character 1: Pinguino [51] and Character 2: Oti [50]) exhibit distinct NVLink transfer patterns.

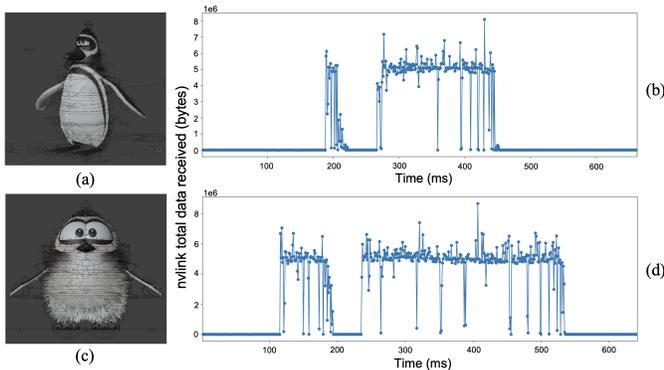


Figure 11: The NVLink leakage traces for two 3D characters from Blender Studio: (a) Character 1: Pinguino [51], (b) the NVLink leakages for Pinguino, (c) Character 2: Oti [50], and (d) the NVLink leakages for Oti.

Experimental setup and data collection. Similar to our application fingerprint attack, the background spy program profiles the values of the specific counters: `nvlink_total_data_received`, as well as timing delays resulting from the victim application’s contention on NVLink. Our evaluation of the attack was conducted on the public cloud machine (a GCP 2-V100 machine). We discovered that Blender does not support configurations with 4-V100 or 8-V100

on GCP, as each pair of GPUs requires an NVLink connection. However, as depicted in Fig. 1b, the GCP GPU machine’s ring topology does not fit for 4 or 8 GPUs. For victim 3D characters, we select 50 fully rigged characters from the Blender Studio open movies [8]. Each character is rendered within the exact same background scene with the same camera angle and resolution. We split the dataset into training and testing using an 80/20 ratio.

Feature engineering and classification. Similarly, we exploit a sliding window approach with a window size of 200 to extract the same 12 time-series features as our application fingerprint attack. We then utilize KNN, XGBoost, and LightGBM models to infer which 3D character the victim renders. As shown in Table 7, LightGBM obtains the highest F1 score (86.86%) when relying solely on contention-based timing leakage, with XGBoost following closely at 85.30%. When performance counters are included, both XGBoost and LightGBM see further improvements, reaching F1 scores of 90.11% and 91.56%, respectively.

Table 7: 3D graphics character fingerprint performance: F1 (%), Precision (%), and Recall (%) on GCP (2 GPUs). ⌚ = Contention-based timing leakage, 📊 = Leaky performance counters.

		F1	Prec	Rec
⌚	KNN	61.37	63.21	64.50
	XGBoost	85.30	87.70	85.50
	LightGBM	86.86	88.99	87.00
⌚ + 📊	KNN	59.74	62.71	62.50
	XGBoost	90.11	93.10	90.50
	LightGBM	91.56	94.11	92.00

7 Cross-VM Attack

During reverse engineering exercises, we found a surprising observation: NVLink counters expose visible leakage across GPUs that do not communicate directly, provided that there is a link connecting them (this link is not in use). This potentially enables GPUs belonging to different VM instances to observe leakage across instances. In this section, we first demonstrate and characterize this leakage between two VM instances on GCP. We then implement the 3D rendering fingerprinting side channel attack across the two VM instances using this leakage.

Prerequisite for this attack. The prerequisite for this attack is co-location, meaning the attacker must reside on the same physical host as the target victim. Previous research has extensively demonstrated co-location attacks in cloud systems [16, 45, 66, 67]. Specifically, Zhao et al. [66, 67] presented lightweight and highly successful co-location attacks on Google Cloud Run. Based on these findings, we assume that the attacker has successfully co-located on the same physical GPU instance as the victim. The attacker then exploits NVLink leakages to exfiltrate sensitive information.

Experiment 4: Cross-VM leakage on the GCP. We assume the attacker is already co-located with the victim on the same physical host. To create co-located VMs, we first obtain a 4-V100 GPU instance on GCP, then we create two VMs within it using KVM (Ubuntu 20.04 host), assigning two GPUs to each VM. As shown

in Fig. 12 (a), the victim’s VM instance (Instance 0) includes GPUs 0 and 1, while the spy’s VM instance (Instance 1) contains GPUs 2 and 3. NVLink is used as the interconnect in this topology. All experiments are conducted on the GCP Compute Engine in the us-west1-a region. All experiments were conducted within controlled environments, ensuring our research activities did not impact external public users.

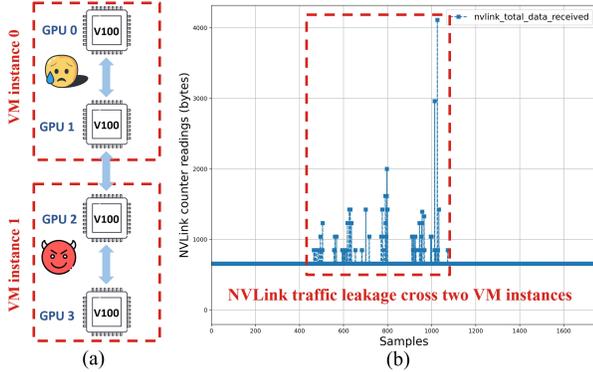


Figure 12: Cross-VM Leakage: (a) Instance topology: Victim resides in VM Instance 0, while the spy operates in Instance 1; (b) NVLink leakage: Leakage across the two VM instances collected from GPU 2 in controlled by the spy’s VM instance.

In this experiment, the victim uses Blender to render 2D images from 3D holograms. The 3D object data is transmitted between GPU 0 and GPU 1 via NVLink. Simultaneously, the spy in another VM instance monitors the NvLink counter (`nvlk_total_data_received`) on GPU 2. As shown in Table 1, each V100 GPU is equipped with six NVLink slots, three of which are connected to peer GPUs. This allows GPU 2 in the spy’s VM instance to monitor NVLink traffic patterns on the link between GPU 1 and GPU 2.

We observe that when two VM instances are connected, the spy can track NVLink traffic patterns from another VM instance by observing performance counters. Figure 12 (b) depicts the NVLink traffic leakages collected across the two VM instances. The signal measured on GPU 2, does not reflect the full traffic between GPU 1 and GPU 0, but it is correlated to it, providing consistent patterns for the different Blender characters. This pattern can be observed as the sequence of spikes in the middle are caused by the program execution occurring within the victim’s VM instance 0.

Observation 6: When two VM instances are connected via NVLink, NVLink counters leak traffic patterns across VM instances even though this traffic does not occur on the physical link connecting the instances.

Attack 3: identifying rendered 3D characters across VMs. In this attack, we investigate whether the attacker can identify the 3D character the victim is rendering in a cross-VM scenario. Similar to our second attack, the background spy program monitors specific performance counters, including `nvlk_total_data_received`, along with timing delays. The victim renders 50 fully rigged 3D

characters from the Blender Studio open movies. Each character is rendered in the same background scene, using the same camera angle and resolution. The dataset is split into training and testing sets using an 80/20 ratio.

Feature engineering and classification. Similarly, we use a sliding window approach with varied window sizes ranging from 100 to 1000 to extract the same 12 time-series features as in our application fingerprint attack. We then apply KNN, XGBoost, and LightGBM models (using the same hyperparameter settings as in Attack 2) to infer which 3D character the victim is rendering. Figure 13 presents the performance (F1 scores) of the three classifiers for different window sizes. We observe that with a window size of 1000, the LightGBM achieves the best performance, with an F1 score of 88.57%, a precision of 91.16%, and a recall of 88.50%.

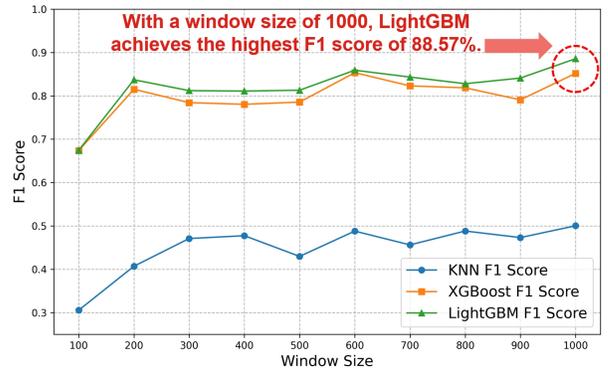


Figure 13: F1 scores with different window sizes.

8 Potential Mitigations

We discuss three potential classes of mitigations: (1) managing access to leaky counters, (2) restricting access to high-resolution clock timing instructions, and (3) detecting abnormal NVLink monitoring and/or contention.

Managing access to counters. Reducing the sampling rate of performance counters may diminish the effectiveness of the spy application [34, 63]. However, this approach could negatively impact legitimate users, as the functionality of these counters may not operate correctly. Fig. 14 presents the impact of reducing the sampling rate on 3D character classification. Although the sampling rate is reduced to 1 Hz, the attacker can still gain information about the 3D character with an F1 score exceeding 40%, significantly outperforming a random guess (2%). We conjecture that even when the sampling rate is restricted to low levels, the leaky counters continue to retain valuable signals that assist attackers in inferring the activities of other users.

Completely blocking access to NVLink counters appears to be a viable defense against *NVBleed*. However, our findings indicate that *NVBleed* remains feasible even when attackers solely exploit timing characteristics to estimate communication behavior (e.g., Equation 1). Using these estimated values, we retrained the models for a 3D character fingerprint attack: we were able to accurately identify the correct 3D character, achieving an F1 Score of over 83%

with the LightGBM model even when performance counters are not accessible.

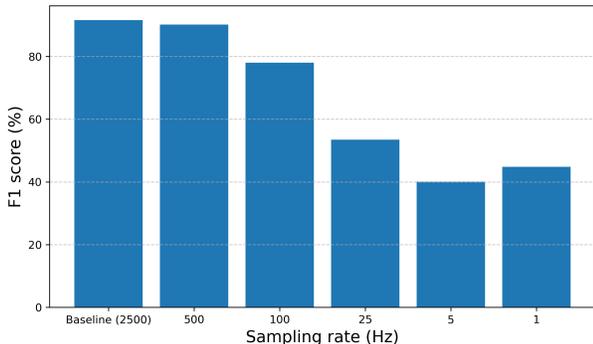


Figure 14: Accuracy with reduced sampling rate.

Restricting access to high-resolution clock instructions. Our attacks utilize the high-resolution clock instruction, *RDTSCP*, to measure the victim’s contention on a shared NVLink. Completely blocking access to these clock instructions could deter our attacks; however, legitimate users may also require such instructions to evaluate the performance of their programs. On the other hand, even if specific clock instructions are prohibited, attackers can still utilize alternative low-requirement clock instructions (e.g., Timer interrupts [46]) or create a synthetic timer, as discussed in [13].

Detecting abnormal NVLink monitoring and/or contention. *NVBleed* operates by creating contention on shared NVLink interconnects and continuously probing the NVLink. A potential defense involves monitoring for such suspicious NVLink querying behaviors. GPUGuard [61] proposes a contention detection and dynamic partitioning framework designed to defend against covert and side channels in GPUs. However, their method primarily safeguards applications on a single GPU and is incompatible with multi-GPU systems. Additionally, the current hardware of NVLink does not support their methods of dynamic partitioning.

9 Related Work

Covert and Side-attacks in GPUs. Covert and side-channel attacks have been extensively studied in discrete GPUs. Naghibijouybari et al. [33] introduced a contention-based covert channel across various GPU resources. Subsequent work conducted multiple side-channel attacks on both graphics and computational GPU workloads by monitoring GPU performance counters [34, 60]. Ahn et al. [1] proposed a timing covert channel for GPUs that exploits the shared, on-chip interconnect channels. Additionally, Nayak et al. [35] developed a covert channel leveraging the GPU’s shared last-level translation lookaside buffer (TLB).

Recent studies also have highlighted several covert and side-channel attacks on integrated GPUs. Dutta et al. [12] demonstrated covert and side-channel attacks between CPUs and GPUs through the shared Last Level Cache (LLC) and ring bus in integrated CPU-GPU systems. Yang et al. [62] present a side-channel attack on mobile GPUs to eavesdrop on user credentials via GPU performance counters. Almusaddar et al. [2] exploited observable slowdown in

shared read and write buffers within the memory controller and constructed a cross-processor covert channel in integrated CPU-GPU systems. Wang et al. [58] identified a side-channel leakage during the graphical data compression process on integrated GPUs. **Interconnect contention based attacks.** Our attacks can also be classified as interconnect contention-based attacks. Previous research has shown that such leakages can be exploited to create covert and side channels. Tan et al. [53] introduced PCIe congestion side-channel attacks that span GPUs, Network Interface Cards (NICs), and Solid-State Drives (SSDs). Similar contention-based attacks have been executed on other hardware architectures, such as the Last Level Cache (LLC) [31], CPU ring bus [42], the Host-GPU PCIe bus [47], and the CPU Mesh [9, 57]. These prior attacks share a high-level observation with our attack: traffic from different sources on shared interconnects induces measurable contention. However, beyond this high-level similarity, our attack differs in several key aspects. Firstly, since we target multi-GPU systems, the threat model and attacker co-location options are significantly different. Prior attacks primarily focus on interconnects within a single CPU or GPU, requiring the attacker to co-locate with the victim. In contrast, our attack exploits inter-GPU communication, differing from traditional co-location, as the attacker can reside on a different GPU or even in a separate VM instance. Secondly, prior attacks typically exploit interconnects carrying cache traffic, memory transactions, or I/O operations, whereas our attack targets inter-GPU traffic. This distinction influences both the type of leakage exposed and the methodology for constructing end-to-end attacks. Beyond intra-VM attacks, our work demonstrates a cross-VM attack on a public cloud provider (GCP) and identifies a new leakage.

The only prior work on microarchitectural attacks in multi-GPU systems is by Dutta et al. [13], which employs prime-and-probe techniques to create cache contention via pinned memory pages. However, our attack differs in several key ways: (1). Communication-based leakage: We observe communication behavior rather than memory access patterns, revealing complementary leakage that can be combined for more powerful attacks. (2). No co-location requirement: Our attack does not require co-location, allowing an attacker to be on a remote GPU (even in a different VM instance) while still monitoring communication traffic between GPUs. By demonstrating the first attack on communication across multi-GPU interconnects, we expand the scope of contention-based side-channel research. This work highlights new security risks in multi-GPU systems and extends the side-channel threat model beyond traditional cache and memory-based attacks.

Cross-VM attacks. Groups of works have demonstrated the cross-VM attack on cloud systems. Ristenpart et al. [45] conducted the first study on co-residence detection in commercial cloud servers. Fang et al. [16] showed how attackers could manipulate cloud schedulers to achieve high co-location rates with target victims. Recently, Zhao et al. [66, 67] conducted co-location attacks in public cloud systems and successfully implemented an end-to-end LLC Prime+Probe side-channel attack on Google Cloud Run.

10 Concluding Remarks

In this paper, we demonstrate covert and side-channel attacks on multi-GPU interconnects. Through reverse engineering, we identify the communication patterns of two generations of NVLink. We develop two main classes of leakage vectors within NVLink: contention-based timing delays and leaky NVLink counters. Additionally, we demonstrate five specific attacks: two covert channels, two end-to-end side-channel attacks across multiple GPUs, and one side-channel attack across VMs. We believe the vulnerability of communication-based leakage might exist in other interconnected systems including other multi-GPU (and even multi-accelerator) systems, with different interconnects and potential leakage sources.

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